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Shunpei YAMAZAKI et al.	)	
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For: SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME	)	

VERIFICATION OF TRANSLATION

Honorable commissioner of patents and Trademarks
Washington, D.C. 20231

Sir:

I, Ikuko Noda, 3-G, 1551, Hase, Atsugi-shi, Kanagawa-ken 243 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 3-135569 filed on May 11, 1991; and

that to the best of my knowledge and belief the following is a true and correct translation of the Japanese Patent Application No. 3-135569 filed on May 11, 1991.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 24th day of April , 1997

Ikuko Noda

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[Title of the Invention] An Insulating Gate Type Field Effect Semiconductor Device and a Manufacturing Method Thereof

[Number of Claims] 8

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[List of Attachment]
[Attachment] Specification 1
[Attachment] Drawing 1
[Attachment] Abstract 1

[Name of Document] Specification

[Title of the Invention] An insulating gate type field effect semiconductor device and a manufacturing method thereof

[Claims]

[Claim 1] An insulating gate type field effect semiconductor device provided on a substrate, said insulating gate type field effect semiconductor device wherein an insulating film of material of a gate electrode is provided around the gate electrode; the electrode connecting source, drain regions touches the upper and side surfaces of said source, drain region; said electrode connected to said source, drain extends to said insulating film provided around said gate electrode.

[Claim 2] An insulating gate type field effect semiconductor device provided on a substrate, wherein an anodic oxide film of aluminum forming a gate electrode is provided around the gate electrode; the aluminum electrode connecting said source, drain region touches the upper and side surfaces of said source, drain region; a semiconductor layer provided under said gate electrode is penetrated at the portion of only the upper and side surfaces touched by said aluminum electrode from the end face portions of said gate electrode and said anodic oxide film.

[Claim 3] A method of manufacturing an insulating gate type semiconductor device comprising the steps of: forming a semiconductor film on a substrate with an insulating surface; forming a gate insulating film on said semiconductor film; forming a gate electrode on said gate insulating film and thus processing the gate electrode in a decided pattern by utilizing a mask; forming an anodic oxide film around the gate electrode at least near the channel formation region by performing an anodic oxidation to said gate electrode after said process; forming a film on said anodic oxide film followed by leaving this film by anisotropic etching near the side wall of an elevated portion formed by said anodic oxide film and said gate electrode; removing said gate insulating film and said semiconductor film by etching, by using said residual region and said elevated region as a mask; exposing said semiconductor film outside of said elevated portion by removing said residual portion by etching; after forming a film for an electrode of the source, drain region touching said exposed semiconductor film, forming source, drain electrode extending to

said anodic oxide film by patterning said film for an electrode by utilizing a mask.

[Claim 4] An insulating gate type semiconductor device comprising the steps of: forming a semiconductor film on a substrate with an insulating surface; patterning said semiconductor film at a decided region like an island by utilizing a mask; forming a gate insulating film on said semiconductor film forming a gate electrode on said insulating film and thus processing the gate electrode in a decided pattern by utilizing a mask; forming an anodic oxide film around the gate electrode at least near the channel formation region by performing anodic oxidation to said gate electrode after said process; forming a film on said anodic oxide film followed by leaving this film by anisotropic etching near the side wall of an elevated portion formed by said anodic oxide film and said gate electrode; removing said gate insulating film and said semiconductor film by etching, by using said residual region and said elevated region as a mask; exposing said semiconductor film outside of said elevated portion by removing said residual portion by etching; after forming a film for an electrode of the source, drain region touching said exposed semiconductor film, forming source or drain electrode separately on said anodic oxide film by patterning said film for an electrode by utilizing a mask.

[Claim 5] A method of manufacturing an insulating gate type field effect semiconductor device of claim 3, comprising a process of doping impurities to the source, drain region after etching said semiconductor film so that it is exposed from said elevated portion by utilizing said elevated portion and said residual portion as a mask.

[Claim 6] A method of manufacturing an insulating gate type field effect semiconductor device of claim 4, comprising a process of doping impurities to the source, drain region after etching said semiconductor film so that it is exposed from said elevated portion by utilizing said elevated portion and said residual portion as a mask.

[Claim 7] A method of manufacturing an insulating gate type field effect semiconductor of claim 3, comprising the step of doping impurities to a region not covered with said anodic oxide film after the step of forming an anodic oxide film around said gate electrode.

[Claim 8] A method of manufacturing an insulating gate type field effect semiconductor device of claim 4, comprising the step of doping impurities to a region not covered with said anodic oxide film after the step of forming an anodic oxide film around said gate electrode.

[Detailed Description of the Invention]

[0001]

[Field for Industrial Use]

The present invention relates to a thin film transistor, and is especially applicable to a liquid crystal electro-optical device, a contact type image sensor device, and the like.

[0002]

[Prior Art]

The insulating gate type field effect semiconductor devices conventionally known have been widely utilized for various fields. This semiconductor device is formed on a silicon substrate, and utilized as an IC or LSI by mechanically integrating many semiconductor devices.

[0003]

On the other hand, thin film type insulating gate type field effect semiconductor device (hereinafter called as TFTs) formed by depositing a thin film not only on a silicon substrate but on an insulating substrate and the like is getting utilized attentively for a switching device portion of a picture element of a liquid crystal electro-optical device, a portion of a driving circuit, and a read-out circuit element of contact type image sensor.

[0004]

Because the TFTs are formed by depositing thin films on an insulating substrate by a gas phase method as above mentioned, it can be formed under a low formation atmosphere temperature up to 500°C. Inexpensive soda glass and borosilicate glass can be utilized as a substrate.

[0005]

In this way, the TFTs can be formed on an inexpensive substrate, and the maximum size of it is only limited to the size of an apparatus which forms a thin film by a gas phase method, and transistors can be formed easily on a large-area substrate. Therefore, use for a liquid crystal electro-optical device in a matrix structure with many picture elements and for one-dimensional or two-dimensional image sensor is expected. And it is partly realized.

[0006]

A representative structure of the TFTs is schematically shown in Fig. 2.

[0007]

In Fig. 2, reference numeral 1 is an insulating substrate comprising glass, 2 is a thin film semiconductor comprising an amorphous semiconductor, 3 is a source, drain region, 7 is a source, drain electrode, and 11 is a gate electrode.

[0008]

Generally, such TFTs are formed by forming a semiconductor film on a substrate, and then by patterning this semiconductor region 2 like an island to needed portions, by utilizing the first mask. Nextly, this gate insulating film 6 is formed, and a gate electrode material is formed on this, and a gate electrode 11 and a gate insulating film 6 are patterned by the second mask.

After that, a source, drain region 3 is formed on a semiconductor region 2 in self-aligned manner with a photo resist mask formed by the third mask and the gate electrode 11 as masks. After that, an interlayer insulating film 4 is formed. A contact hole is formed by the forth mask on this interlayer insulating film for electrode connection to source, drain region 3. After that, after formation of the material of the electrode, this electrode material is performed with patterning by the fifth mask and an electrode 7 is formed. Thus TFTs are completed.

[0009]

[Problems the present invention intends to solve]

Like this, TFTs utilized five masks in general, and complemental TFTs needed six masks. Naturally, more masks are needed to make a complicated integrated circuit. Use of many masks like this needs complicated processes in a process of manufacturing TFTs, and the number of mask alignment naturally increases. This causes decrease of yield and productivity of manufacturing TFT devices. Moreover, enlarging of electric devices utilizing TFT elements and downsizing of TFT element itself, and minuting of the pattern were cause of decreasing them further. Thus process which does not need complicated processes and a structure of new TFTs decreasing the number of masks needed for manufacturing TFTs were expected.

[0010]

The present invention relates to a new structure and simple process of an insulating gate type field effect semiconductor device. Compared with the prior art, TFTs can be formed with less masks.

[0011]

[Means to solve the problems]

Anodic oxide films of a material comprising a gate electrode is provided around the gate electrode of TFTs of the present invention, and the electrode connecting the source, drain region touches the upper and side faces of said source, drain region, and said electrode connected to source, drain extends over the upper portion of said oxide film provided around said gate electrode.

[0012]

That is, as is shown in a schematic figure of TFTs of the present invention shown in Fig. 1, an anodic oxide film 10 is provided at least around the gate electrode 8, and upper face and side face of the source, drain region 3 is penetrated a little from the end face of this anodic oxide film, and the electrode 7 is connected the source, drain region at this penetrated portion and occupies the connected area largely. Moreover, this electrode 7 is extended over the anodic oxide film 10 and is performed with patterning at this portion, and separated to each electrode.

[0013]

Fig. 3 schematically shows a process of forming TFTs of a structure like in Fig. 1. Figures shown in this specification simply shows a schematic idea for explanation, so it is different from the actual size and form. An example of a manufacturing process of TFTs of the present invention is shown in Fig. 3.

[0014]

First of all, like Fig. 3(A), a semiconductor layer 2 is formed on grass substrate for example, a crystallizing glass 1, which has heat resistance. As this silicon semiconductor layer, a wide variety of semiconductors such as amorphous semiconductor, poly-crystal semiconductor can be utilized. As a manufacturing method, plasma CVD method, sputtering method, or heat CVD method and the like can be selected depending on the type of adapted semiconductor. Here, the following process will be explained with a poly- crystal silicon semiconductor.

[0015]

A silicon oxide film 6 to be a gate insulating film is formed on this semiconductor layer 2. Moreover, a material for an electrode to be a gate electrode, here aluminum as a material for an electrode, is formed on this. After that, this gate electrode 8 is performed with patterning by the first mask 1. After this, peripheral portion of this gate electrode 8 is performed with anodic oxidation, and non-porous aluminum oxide 10 is

formed at least around the channel region like Fig. 3(B).

[0016]

As a solution utilized for this anodic oxidation, typically strong acid solution like sulfuric acid, nitric acid, phosphoric acid, and mixed acid like citric acid mixed with ethylene glycol, propylene glycol can be utilized. According to necessity, it is possible to mix salt or alkali solution to control pH of this solution.

[0017]

First of all, the substrate is dipped in AGW electrolyte added with propylene glycol and tartaric acid solution by 9:1. The aluminum gate electrode is connected to the anode of an electrode, and DC current is applied by utilizing platinum as a cathode.

[0018]

Condition of anodic oxidation is sending of current of $3mA/cm^2$ current concentration for 20 minutes by constant current mode, and 5 minutes of constant voltage mode. Thus aluminum oxide of 1500Å thickness is formed around the gate electrode. Insularity of this aluminum oxide was studied by the sample made by the same condition as this oxidation. It is an aluminum oxide film with resistivity of $10^{15}\Omega$, and insulating pressure of $3 \times 10^6 V/cm$.

[0019]

The surface of this sample is observed by scanning electron microscope with approximately 10,000 magnification. It is uneven on the surface, but is a good insulating film without minute holes.

[0020]

After a silicon oxide film 12 is formed upside of this by plasma CVD, anisotropic etching is performed from this condition to the substrate in almost vertical direction, and silicon oxide 13 is left on the side of the elevation comprising a gate electrode and anodic oxide film like in Fig. 3(D). After that, the semiconductor layer 2 is removed by etching of self-aligned manner with mask of the silicon oxide 13, the gate electrode 8 and anodic oxide film 10 in the elevation. Fig. 3(E) shows this procedure. The condition of the upper surface is shown in Fig. 4(A). Cross section A-A' in Fig. 4 is shown in Fig. 3.

[0021]

After this condition, the silicon oxide film 13 and the gate insulating film are removed by selectively etching silicon oxide with the gate electrode 8 and its anodic oxide film 10 as a mask. A part of the semiconductor layer 2 is exposed from the end portion of the gate

electrode like Fig. 3(F) and Fig. 4(B).

[0022]

Nextly, impurity is doped to this exposed portion so that this would become source, drain region. As is shown in Fig. 3(F), phosphorous ion is hit from the upper side of the substrate with the anodic oxide film 10 of the gate as a mask. In this way, source, drain region 3 is formed. After that, to activate the region, laser is irradiated there, and the source, drain region is activated by laser annealing. For this activation, heat annealing and the like can be utilized.

[0023]

After that, aluminum to be electrodes of source, drain is formed on this, and electrodes of source, drain are separated by etching the electrode of source, drain in a decided pattern with the second mask 2. This condition is shown in Fig. 4(C). Finally, the penetrated semiconductor layer 2 is removed by etching with electrodes 7 of source, drain and the anodic oxide film 10 of gate electrode as a mask, and TFTs shown in Fig. 3(G) and Fig. 4(D) are obtained.

In this way, the present invention can make TFTs by just two masks.

In addition, if the TFTs are made in complemental structure, it is possible to make them with 1 to 2 additional masks.

[0024]

Contact from outside to the gate electrode is achieved by forming an anodic oxide film by making a part of the gate electrode not touched to electrolyte for anodic oxidation, or by removing the anodic oxide film exposed to outside by selective etching of the source, drain electrode and the anodic oxide film after etching the unnecessary semiconductor film finally. Of course, it is possible to contact by opening holes for contact to specific anodic oxide film with the third mask.

[0025]

In the above mentioned explanation, the manufacturing process of TFTs is just an example, and is not limited to the manufacturing method explained in this example. For example, the process of doping impurities in the source, drain region is performed after patterning of the semiconductor layer 2 as is shown in Fig. 3(F), but it is also possible to perform ion hitting with the anodic oxide film 10 of the gate as a mask in a condition shown in Fig. 3(B).

[0026]

In the state after formation of the semiconductor layer 2 and before formation of a gate electrode, if the semiconductor layer is performed with

patterning only at the region of the TFTs like an island as is shown in Fig. 5, the semiconductor layer 2 does not exist under the lead wiring of the gate electrode, and there is only the substrate or the insulating film on the substrate. At this portion, it is possible to make the gate electrode wiring and the condenser not exist. With this structure, it is possible to form TFTs which can response faster by three masks. The state of the upper face of this is shown in Fig. 5(A), and B-B' cross section of the figure of the upper face is shown in Fig. 5(B).

[0027]

[Example]

[Example 1]

This example is an example of application of the TFTs of the present invention for an active matrix type liquid crystal electro-optical device with the circuit structure shown in Fig. 6. As is apparent from Fig. 6, the active element of this example is in complemental structure, and PTFTs and NTFTs are provided to each pixel electrode.

Fig. 8 shows the structure of arrangement of electrodes and the like corresponding to this circuit structure. To make explanation simple, the portion corresponding to 2 x 2 is only shown.

[0028]

The method of manufacturing the substrate for a liquid crystal electro-optical device utilized in this example is explained in Fig. 7. In Fig. 7 (A), a silicon oxide film as a blocking layer 51 is formed by 1000-3000Åthickness on a glass 50 such as quartz glass which is inexpensive and can bear heat of 700°C or less, such as approximately 600°C. The process condition is an oxygen atmosphere of 100%, deposition temperature of 15°C, output of 400-800W, and pressure of 0.5Pa. The deposition speed when quartz or single-crystal silicon is utilized as a target is 30-100Å/minute.

[0029]

A silicon film 52 was formed on this by LPCVD (low pressure gas phase) method, sputter method or plasma CVD method. If it was formed by low pressure gas phase method, deposition was performed by providing disilane (Si_2H_6) or trisilane (Si_3H_8) to a CVD apparatus at 450-550°C which is lower than the crystallizing temperature by 100-200°C, such as 530°C. The pressure inside the reaction furnace was made as 30-300Pa. The deposition speed was 50-250Å/minute. To control the threshold voltage (Vth) of PTFTs and NTFTs approximately the same, boron can be added by utilizing diborane during deposition by 1 x 10^{15} -1

x $10^{18}cm^{-3}$ concentration.

[0030]

If sputter method is utilized, a background pressure before sputtering was made as 1 x 10^{-5}Pa or less, and single-crystal silicon was utilized as a target, and was performed in an atmosphere of argon added with hydrogen by 20-80%. For example, argon was 20%, and hydrogen was 80%. The deposition temperature was 150°C, frequency was 13.56MHz, and sputtering output was 400-800W. Pressure was 0.5Pa.

[0031]

If a silicon film is formed by plasma CVD method, temperature was situated as 300°C for example, and monosilane (SiH_4) or disilane (Si_2H_6) was utilized. This was introduced in a PCVD apparatus, and deposition was performed by adding high frequency power of 13.56MHz.

[0032]

It is desirable if the film formed by this method has oxygen concentration of 5 x $10^{21}cm^{-3}$ or less. If concentration of this oxygen is high, a semiconductor layer is difficult to be crystallized, so that heat annealing temperature should be made higher or the time of heat annealing should be made longer. If the oxygen concentration is too little, leak current of off condition increases by back light. So it is made as 4 x 10^{19} to 4 x $10^{21}cm^{-3}$. The amount of hydrogen is 4 x $10^{20}cm^{-3}$, and is approximately 1 atom% compared with 4 x $10^{22}cm^{-3}$ of silicon. To accelerate crystallization of the source, drain, oxygen concentration can be made as 7 x $10^{19}cm^{-3}$ or less, desirably 1 x $10^{19}cm^{-3}$ or less. Oxygen can be added only to the channel formation region of TFTs comprising a pixel by ion injection method so that it becomes 5 x 10^{20} - 5 x $10^{21}cm^{-3}$. It is effective to decrease contamination of oxygen less and to make the TFTs have higher carrier mobility to make high frequency operation, because light is not irradiated to the TFTs forming the peripheral circuit.

[0033]

By above mentioned method, after making a silicon film of amorphous condition by 500 to 3000Å thickness, for example 1500Å, it is heated at a medium temperature at 450 to 700°C in non-oxide atmosphere for 12 to 70 hours, for example, at 600°C in hydrogen atmosphere. Because a silicon oxide film of amorphous structure is formed on the substrate surface under the silicon film, a specific core does not exist by this heating, and the entire portion is equally treated with heat annealing. That is, there is an amorphous structure during deposition, and hydrogen is merely contaminated.

[0034]

By annealing, the silicon film is changed from amorphous structure to a state with high regularity. A part of it is crystal, and the carrier mobility obtained is hole mobility(μh)=10-200cm^2/VSec, electron mobility (μe) = 15 - 300cm^2/VSec.

[0035]

In Fig. 7(A), a silicon film is performed with photo etching by the first photo mask 1, a region 30 for PTFTs (channel width of 20μm) is formed in the left side of the figure, and a region 40 for NTFTs is formed in the right side.

[0036]

On this, a silicon oxide film is formed by 500-2000Å thickness, for example, 700 Å, as a gate insulating film 53. This is in the same condition as that of formation of a silicon oxide film 51 as a blocking layer. A little amount of fluoride can be added during deposition to fix sodium ions. In this example, a silicon nitride film 54 is formed by 50-200Å such as 100Å on this silicon oxide film as a blocking layer to control reaction between the gate electrode formed on this and the gate insulating film.

[0037]

After this, aluminum is formed by 3000Å-1.5μm, for example 1μm thickness, on it as a material for a gate electrode, by the known sputtering method.

As this gate electrode material, molybdenum(Mo), tungsten(W), titanium(Ti), tantalum(Ta), alloy of these materials mixed with silicon, or deposited wirings of metal film can be utilized.

[0038]

If a metal material is utilized as a gate electrode like in this example, especially in the case of low resistance material such as aluminum, increase of gate delay (delay of voltage pulse running through the gate wiring and distortion of waveform) produced by the large area and high resolution of the substrate can be suppressed. Thus enlargement of the substrate can be easily performed.

[0039]

This is performed with patterning by the second photo mask 2 , and Fig. 7(B) is obtained. A gate electrode 55 for PTFTs, and a gate electrode 56 for NTFTs are formed. Both of these electrodes are connected to the same gate wiring 57.

[0040]

This substrate is dipped in AGW electrolyte added with propylene

glycol and tartaric acid solution by 9:1. The aluminum gate electrode is connected to the anode of an electric source, and DC current is applied by utilizing platinum as a cathode. Here, the gate electrodes are connected by each of their gate wiring, and connecting terminals are provided so that they connect all gate wirings by flanking them at the portion near the end portion of the substrate. As in Fig. 7(C), anodic oxide films 58 and 59 are formed around the gate electrode.

[0041]

Condition of anodic oxidation is firstly sending of current of $4mA/cm^2$ current concentration for 20 minutes by constant current mode, and 15 minutes of constant voltage mode. Thus aluminum oxide of 2500Å thickness is formed around the gate electrode. It is better to form this anodic oxide film as thick as possible, so that it is formed thickly to the limit of the process condition.

[0042]

As is shown in Fig. 7(D), after removing a silicon nitride film 54 and a silicon oxide film 53 on the semiconductor by etching, boron is added by dose amount of $1 - 5 \times 10^{15} cm^{-2}$ to the entire substrate as an impurity for PTFTs by ion injection method. This dope concentration is made as approximately $10^{19} cm^{-3}$, and source 60 and drain 61 of PTFTs are formed. In this example, ion doping is performed after removing the surface insulating film. However, if condition of ion hitting is changed, doping can be also performed through insulating films 53, 54 on this semiconductor film.

[0043]

As is shown in Fig. 7(E), after a photo resist 61 is formed by the third photo mask 3 and PTFT region is covered, phosphorous is doped by ion injection method by dose amount of $1 - 5 \times 10^{15} cm^{-2}$ to source 62, drain 63 for NTFTs so that the dope concentration would be approximately $10^{20} cm^{-3}$. During ion doping process as this, the direction of ion hitting is made as diagonal to the substrate, and the end portion of the source, drain region was made approximately at the end portion of the gate electrode, by making impurity go under the anodic oxide film around the gate electrode. By doing this, the anodic oxide film comes to have enough insulating effect to the electrode wiring to be formed in the following process. It becomes unnecessary to form a new insulating film.

[0044]

Nextly, heat annealing is performed again at 600°C for 10 to 50 hours, and the impurity region is activated. Source 60, drain 61 of PTFTs,

and source 62, drain 63 of NTFTs are made as P+ and N+ respectively, by activating the impurity. Channel formation regions 64 and 65 are formed under gate electrodes 55 and 56. In this example, heat annealing is used as this activating process, but a method of activation such as irradiation of laser light to the source, drain region can be also used. In this case, because activation is performed momentary, it is not necessary to think of diffusion of metal material utilized for a gate electrode. It is possible to omit a silicon nitride film 54 for blocking on the gate insulating film utilized in this example.

[0045]

After this, an insulating film is formed on it by said sputter method as a silicon oxide film. The thickness of this film is made as thick as possible, for example, 0.5 to 2.0μm. In this example, it is formed at 1.2μm thickness. Then, anisotropic etching is performed from the upper surface, and a residual region 66 is formed near the side wall of an elevation comprising a gate electrode and an anodic oxide film. This is shown in Fig. 7(F).

[0046]

Unnecessary portion of the semiconductor film 52 is removed by etching with this elevated portion and the residual region 66 as a mask. A semiconductor film 52 to be source, drain region of each TFT is exposed around the elevated portion, as is shown in Fig. 7(G).

[0047]

Aluminum is formed by sputter method on the whole portion of these. After patterning of lead 67, 68, and contact portion 69, 70 by the fourth mask 4 , a semiconductor film penetrated from the electrodes 67, 68, 69,70, and the gate electrodes 55, 56, and the semiconductor film 58, 59 penetrated from anodic oxide film around them is removed by etching. Thus a perfect element separation is performed and TFTs are completed. By the manufacturing method as this, TFTs of a complementary structure can be formed by four masks. This is shown in Fig. 7(H).

[0048]

This TFTs are covered with an anodic oxide film around the gate electrode. The source, drain region is penetrated from the gate electrode portion only at the portion of connecting an electrode. All of the portions other than them exist under the gate electrode. The source, drain electrode is touched with two portions of the upper face and the side face of the source, drain region, and has enough ohmic contact.

[0050]

In this way, even by self-aligned manner, C/TFTs can be formed without heating at 700°C or more in every process. Therefore, it is not necessary to utilize an expensive substrate like quartz as a substrate material, and is a very appropriate process for a large-area liquid crystal display device of the present invention.

[0051]

Heat annealing is performed twice in Figs. 7(A) and (E). However, annealing of Fig. 7(A) can be omitted depending on the required characteristic, and formation time can be shortened by making both of the annealing the annealing in Fig. 7(E). Though aluminum is utilized as a gate electrode in this example, a silicon nitride film 54 is provided under it so that aluminum will not react with the gate insulating film under it, a good interface character can be achieved.

[0052]

As is shown in Fig. 7(I), two TFTs are formed in a complemental structure, and ITO (indium-tin oxide film) is formed by sputter method to connect the output terminal to an electrode of the liquid crystal device as a transparent electrode. This is etched by the fifth photo mask 5, and a pixel electrode 71 is formed. This ITO is formed at a room temperature to 150°C, and is achieved by annealing at 200-400°C in oxygen or atmosphere. In this way, PTFT 30, NTFT 40, and electrode 71 of a transparent conductive film are formed in the same glass substrate 50. Electric character of the obtained TFTs is mobility of 20(cm^2/Vs) and Vth of -5.9(V), for PTFTs, and mobility of 40(cm^2/Vs) and Vth of 5.0(V) for NTFTs.

[0053]

Arrangement of electrodes and the like of this liquid crystal electro-optical device is shown in Fig. 8. The cross section C-C' corresponds to the cross section of the manufacturing process of Fig. 7. PTFT 30 is formed at a cross point of the first signal line 72 and the third signal line 57. PTFT for other pixel is provided to a cross of the first signal line 72 and the third signal line 76 on the right in the same way. On the other hand, NTFTs are provided to a cross point of the second signal line 75 and the third signal line 57. At the cross of other neighboring first signal line 74 and the third signal line 57, PTFT for other pixel is provided. It has a matrix structure like this using C/TFT. PTFT 30 is connected to the first signal line 72 at an electrode of the drain 61, and the gate 55 is connected to signal line 57. Output terminal of source 60 is connected to an electrode 71 of a pixel through a contact.

[0054]

On the other hand, NTFT 40 are connected to the second signal line 73 by an electrode of source 62, and a gate 56 is connected to a signal line 57, and an output terminal of the drain 63 is connected to a pixel electrode 71 through a contact like PTFTs. Other C/TFTs connected to the same third signal line and provided next have PTFT 31 connected to the first signal line 74, and NTFT 41 connected to the second signal line 75. In this way, a pixel 80 is formed by a pixel electrode 71 comprising a transparent conducting film and C/TFTs between(inside) a pair of signal lines 72 and 73. By repeating such structure vertically and horizontally, a liquid crystal electro-optical device with a large area pixel like 640 x 480, 1280 x 960 enlarging 2 x 2 matrix can be made. In addition, the impurity region of TFTs is called as source, drain for explanation. In some cases, it functions differently from the meaning of its name.

[0055]

In this example, the semiconductor film 52 is removed by etching like an island and each TFT device is separated. With this, the portion under the gate wiring other than the TFT region does not have a semiconductor film. The portion under this gate wiring is a substrate or an insulating film on the substrate, and will not form a capacitor of input of the gate at this portion. Thus high speed response can be performed.

[0056]

A liquid crystal electro-optical device is made by utilizing a substrate provided with an active element like this. First of all, a resin having ultraviolet hardenability and being dispersed with nematic liquid crystal of 50 percent by weight in epoxy modified acrylic resin is formed by screen method.

[0057]

The mesh concentration of the screen utilized is 125 meshes by 1 inch, and the emulsion thickness is 15μm. Squeegee pressure is 1.5kg/cm^2.

[0058]

After leveling for ten minutes, 1000mJ energy is applied by high pressure mercury lamp having emitting wavelength of mainly 236nm. The resin is hardened, and a light modulating layer of 12μm thickness is formed.

[0059]

After that, Mo(molybdenum) is deposited by 2500Å by DC sputter method to make this the second electrode.

[0060]

Then, a black epoxy resin is printed by screen method, and baked at 50°C for 30 minutes, and after that, is baked at 180°C for 30 minutes. Thus a protecting film of 50μm is formed.

[0061]

A driving IC of TAB form is connected to the lead on the substrate, and a reflection type liquid crystal display device comprising only a substrate is finished.

In this example, TFTs of a complemental structure is provided to each pixel as an active element. However, it is not necessary to limit to this structure, and more than one sets of TFTs of a complemental structure can be provided. More than one sets of TFTs of a complemental structure can be provided to a pixel divided in more than one.

[0062]

In this way, a liquid crystal electro-optical device provided with an active element to a dispersion liquid crystal is completed. Because the dispersion liquid crystal of this example only needs a sheet of substrate, a light thin liquid crystal electro-optical device can be made at a cheap price, and the effect of a liquid crystal electro-optical device can be made real without a use of a deflecting plate or an orientation film. Therefore, a very bright liquid crystal electro-optical device can be made.

[0063]

[Example 2]

In this example, the present invention is utilized for a liquid crystal electro-optical device provided with a transformed transfer gate TFTs of a complemental structure to a pixel. Manufacturing method of TFTs of the present invention is basically the same as that of Example 1, and the process proceeds almost likely as Fig. 7. However, because C/TFTs of a transformed transfer gate are utilized in this example, the actual configuration of the TFTs is arranged and connected in the position shown in Fig. 10 different from that of Fig. 7.

[0064]

As is shown in Fig. 9, PTFT 95 and NTFT 96 connect the gate to a common gate wiring 91. These connect the source, drain region, and connect them to the other signal line 93. The other source, drain region is also connected commonly to the pixel electrode.

[0065]

The same process shown in Example 1 is proceeded to the process shown in Fig. 7(G). Then, a silicon nitride film 100 is formed by 500 to

2000Å thickness on the upper face of them. And then, the silicon nitride film 100 is treated with anisotropic etching in vertical direction to the substrate, and this silicon nitride film is left on the side wall of the anodic oxide film 101 of the gate. Here, it is not necessary to leave the film equally on the side wall, and it can only be left at least at the gate insulating film near the gate electrode 107 and the semiconductor. When an electrode 102 of source, drain is formed in the following process, this silicon nitride film 100 prevents this metal wiring 102 and the source, drain region 104, 105 from short circuit near the end face of a gate insulating film 103.

[0066]

An interlayer insulating film and a silicon oxide film 106 are formed by 1000Å to 2μm, here 6000Å. After a photo resist is formed on the upper surface, light is exposed from the substrate, and a mask is formed on a gate electrode 107 with the gate electrode as a mask, and an interlayer insulating film 106 is formed on the gate electrode by etching treatment.

[0067]

After this, process of Figs. 7(H) and (I) is commenced, and transformed transfer gate TFTs with arrangement and structure in Figs. 10(A), (B), and (C) are made. An interlayer insulating film 106 is formed. As apparent from Figs. 10(B) and (C), the interlayer insulating film 106 exists on the gate electrode 107 without fail. It features function of enough interlayer insulator at the cross portion of the lead portion of the gate wiring 107 and the lead portion of the source, drain wiring 102 like Fig. 10(A). Generation of wiring capacity can be suppressed at the cross portion of these.

[0068]

In this example, with the same number of masks as Example 1, an active element substrate with TFTs which have less capacity near the wirings and which has small possibility of short circuit at the gate insulating film can be achieved.

[0069]

With this substrate as the first substrate, by using the second substrate on which an opposed electrode and an orientation process layer are formed, STN type liquid crystal is injected between these substrates by known technology of cladding, and an active matrix type STN liquid crystal electro-optical device is formed.

[0070]

In above example, examples applied to a liquid crystal electro-optical device are shown. It is applicable not only to this example, but also to other apparatuses and three-dimensional integrated circuit devices.

[0071]

With the structure of the present invention, TFT devices can be formed by utilizing much less number of masks than before. If a semiconductor product is formed by applying an element of this structure, the manufacturing process became easier with decreasing of masks, and yield of manufacturing was improved. A semiconductor applied device with cheaper cost could be provided.

[0072]

In the present invention, a metal material is utilized as a gate electrode material, and an oxide film is provided on the surface of it by anodic oxidation of this metal material, thus providing a wiring in three dimensional structure having a grade separation. Decrease of frequency character of the device and increase of ON resistance could be prevented by providing only the contact portion for source, drain exposed from the gate electrode by said gate electrode and the oxide film near the electrode to make a feeding point close to the channel.

[0073]

Because aluminum is utilized for a gate electrode, during annealing of the process of forming the element, hydrogen in the gate oxide film can be decreased by changing H_2 to H by catalytic effect of aluminum. Compared with the case of utilizing a silicon gate for interface state (Qss) can be decreased and thus characteristic of an element can be improved.

[0074]

Because source, drain regions of the TFTs were made in self-align, and the position of the contact portion of an electrode for feeding was decided in self-aligned manner, too, area needed for the TFTs is decreased and thus integration can be improved. If it is utilized as an active element of a liquid crystal electro-optical device, the rate of opening of a liquid crystal panel can be improved.

[0075]

An anodic oxide film around the gate electrode is attentively utilized, TFTs of a peculiar structure are suggested, and the number of masks for manufacturing TFTs is 2 at the minimum.

[Brief Description of drawings]

[Fig. 1]

An example of a structure of an element of TFTs of the present

invention.

[Fig. 2]

A structure of an element of conventional TFTs.

[Fig. 3]

A schematic cross section of a manufacturing process of TFTs of the present invention.

[Fig. 4]

An upper surface of a manufacturing process of TFTs of the present invention.

[Fig. 5]

Another example of TFTs of the present invention.

[Fig. 6]

A schematic figure of a circuit when the TFTs of the present invention of a complemental structure are applied for a liquid crystal electro-optical device.

[Fig. 7]

A schematic figure of a manufacturing process when the TFTs of the present invention of a complemental structure are applied to a liquid crystal electro-optical device.

[Fig. 8]

A schematic figure of arrangement on the substrate when the TFTs of the present invention of a complemental structure are applied to a liquid crystal electro-optical device.

[Fig. 9]

A schematic figure of a circuit when the TFTs of the present invention of a complemental structure are applied to a liquid crystal electro-optical device.

[Fig. 10]

A schematic figure showing arrangement on the substrate when the TFTs of the present invention of a complemental structure are applied to a liquid crystal electro-optical device.

[Explanation of Marks]

1..... substrate
2..... semiconductor layer
3..... source, drain region
6..... gate insulating film
7..... source, drain electrode

8..... gate electrode
10.....anodic oxide film
13.....residual region
55.....gate electrode
56.....gate electrode
60.....source
61.....drain
62.....source
63.....drain
66.....residual region
71.....pixel electrode

[Name of the Document] Abstract

[Abstract]

[Purpose] Proposal of TFTs of a new structure.

[Structure] An insulating gate type field-effect semiconductor device and a manufacturing method thereof, with a structure of TFTs wherein an anodic oxide film of a material comprising a gate electrode is formed around the gate electrode; the electrode connecting the source, drain region touches the upper and side face of said source, drain region; said electrode contacting said source, drain region extends over said oxide film provided around said gate electrode; and such manufacturing process is achieved by two masks.

[Selected Figure] Fig. 1